ADVAY LABS

Quantum Architecture Validation Report

Fabrication planning ready

Readiness score: 95 / 100 · Confidence: L3 — Engineering Grade

Run ID: sample-2026-005

Issued: 21 July 2026 at 11:07 am IST

Auto-generated platform report — not independently reviewed by Advay Labs.

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1. Executive summary

Verdict: Fabrication planning ready.

Resource projection fits within healthy thresholds across every checked dimension.

Readiness score: 95 / 100. **Confidence:** L3 — Engineering Grade. Resource projection backed by EM-import / S-parameter evidence; suitable for engineering decisions and fabrication-readiness gating.

Gate summary: 7 passed, 0 warnings, 0 failed (7 total synthesised checks).

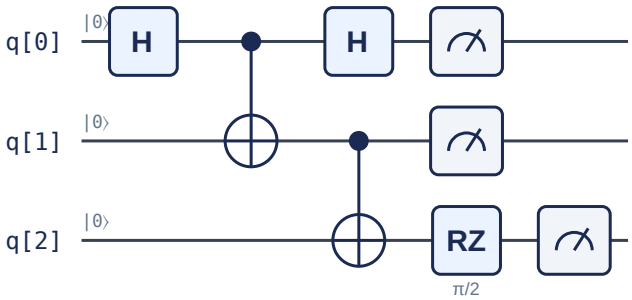
2. Architecture reviewed

Qubits: 8. **Classical bits:** 8. **Depth:** 14.

Gate composition: 17 two-qubit gates, 3 Toffoli-class (3-qubit) gates, 8 measurements.

2A. Input circuit

The submitted circuit uses 3 qubits and 5 operations across 5 time steps, drawn below in standard notation.



Notation: boxes = gates (label, parameter below); ● = control; ○ = negative control; ⊕ = NOT/CX target; ╳ = swap; M = measurement; |0⟩ = initial state; dashed vertical line = spacer between blocks; ⌐ × N ¬ bracket = a loop block drawn once and repeated N times.

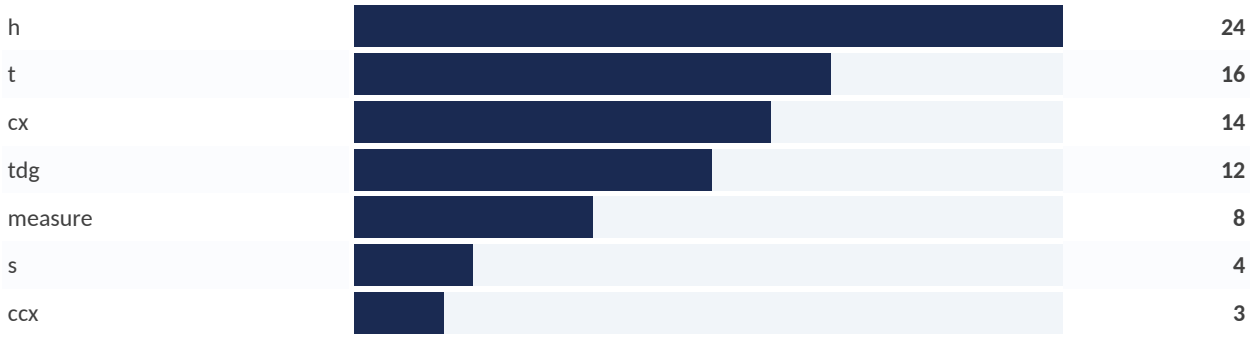
OpenQASM source

```
OPENQASM 2.0;
include "qelib1.inc";
qreg q[3];
creg c[3];
h q[0];
cx q[0], q[1];
cx q[1], q[2];
rz(pi/2) q[2];
h q[0];
measure q[0] -> c[0];
measure q[1] -> c[1];
measure q[2] -> c[2];
```

2B. Visual summary

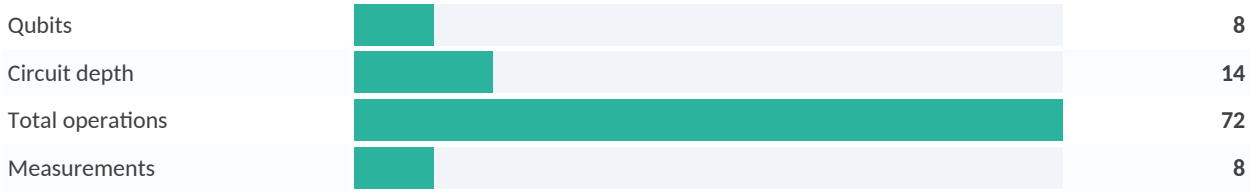
Graphical view of the quantitative results in this report. Exact values appear in the corresponding tables.

Gate composition



Operation count by gate type.

Circuit size



Key circuit dimensions.

End-to-end success probability

Projected success probability by control mode.

3. Resource projection

Quantity	Value	Note
Logical qubits	8	—
Code distance	d = 9	below_threshold_scaling
Physical qubits	188,244	surface_code_litinski_2019
T-count	28	
T-factories	23	invariant: ≤ T-count
Wall clock	0.189 ms	fault-tolerant projection
Fits on SQPU?	**Yes**	

Source: circuit_count_direct.

4. Gate-wise results

The table below shows the per-dimension readiness checks that compose the overall readiness score. Each check carries a weight; the score is the weighted average. Checks scoring ≥ 80 are considered passed, 60-79 are warnings, < 60 are failed.

Check	Score	Status	Note
Fits on SQPU fabric	100	**PASSED**	Yes — projected physical qubits within fabric budget
Physical qubit headroom	100	**PASSED**	188,244 physical qubits projected (healthy ≤ 200,000)
Code distance	100	**PASSED**	d = 9 (healthy)
T-factory allocation	100	**PASSED**	23 factories for 28 T-gates (invariant: factories ≤ T-count = 28)
Wall-clock projection	100	**PASSED**	0.189 ms estimated wall clock
Logical error rate	80	**PASSED**	worst-mode LER = 9.00e-5 per logical cycle
End-to-end success probability	90	**PASSED**	end-to-end success ≈ 97.20% (full control); hybrid 96.10%; reduced 94.80% (degraded control budget)

5. Risk register

No material risks identified at this scope.

6. Recommended engineering actions

Actions are ranked by expected impact on the readiness score. Implementing high-impact items first is generally the most cost-effective path to a fabrication-ready architecture.

- **[LOW IMPACT] Run the full Architecture Validation suite for evidence-grade output —** The playground gives a fast L1/L2 readiness sketch. For evidence-grade output (full 91 gates, sample-immune Monte Carlo, signed report), launch an Architecture Validation run from /dashboard.

7. Readiness scorecard

Overall readiness score	**95 / 100**
Verdict	**Fabrication planning ready**
Confidence	L3 — Engineering Grade
Gates passed	7 / 7

Gates with warnings	0
Gates failed	0

8. Evidence appendix

8.1 Notes from the simulator

- Sample report — illustrative content. Actual run output will differ.

9. Noisy execution comparison (Module 3)

Not available for this run. The noisy-trajectory simulator was either disabled (Fast iteration / Minimal preset) or the circuit exceeded the trajectory cap (22 qubits for the bounded-noise model). Re-run with Full analysis preset on a circuit at or below the cap to populate this section.

10. Noise projection — logical error & end-to-end success

Analytic QEC projection (mwpm_phenomenological). For each control mode the table gives the per-cycle logical error rate and the end-to-end success probability that results from composing (1 − LER) over the projected runtime. End-to-end success is the headline gate that drives the verdict, since a healthy per-cycle LER can still compose to a low success probability over a long circuit. Physical error rate p_phys = 1.00e-3.

Control mode	Logical error / cycle	End-to-end success
full	4.20e-5	97.20%
hybrid	6.10e-5	96.10%
reduced	9.00e-5	94.80%

Intervals are 95% bounds where the projector reports them. Modes: full = all controls active; hybrid = partial; reduced = minimal control budget.

Sensitivity to control reduction: 0.120 (engine LER-sensitivity index). In end-to-end terms, success goes from 97.20% at full control to 94.80% at reduced control — a 2.40 percentage-point drop, driven by the longer QEC cycle time under control reduction.

11. Output distribution

No measured output distribution was produced for this run (execution may have been disabled, the circuit had no measurements, or it exceeded the statevector-execution cap).

12. Run metadata and audit log

Run ID: sample-2026-005.

Status: succeeded.

Evidence classification: stitched_composition.

Simulator version: v43_0_54_2_4_hardware_readiness_preflight

Seed: sample

End of report. Auto-generated platform report — not independently reviewed by Advay Labs. For an Advay-engineer-reviewed report bearing the Advay-reviewed Quantum Architecture Validation Report mark, request the Expert Review add-on at https://advaylabs.com/pricing.